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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03L 7/00 — A2

(11) International Publication Number: **WO 98/58451**

(43) International Publication Date: 23 December 1998 (23.12.98)

(21) International Application Number: PCT/IB98/00589

(22) International Filing Date: 20 April 1998 (20.04.98)

(30) Priority Data:
97201870.9 19 June 1997 (19.06.97) EP
(34) Countries for which the regional or international application was filed: NL et al.

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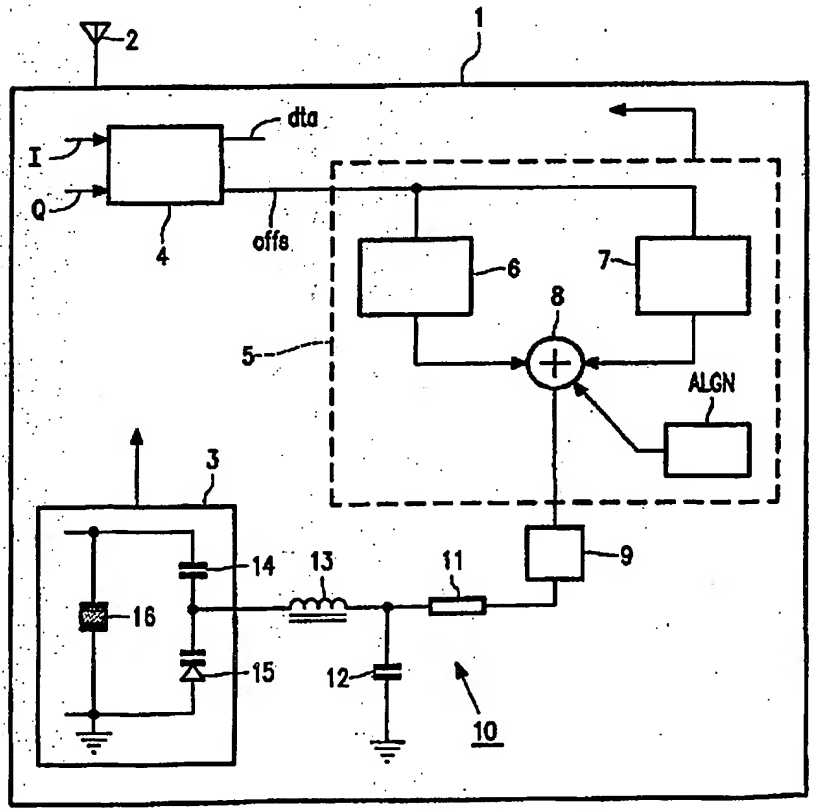
(81) Designated States: CN, JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: DIGITAL COMMUNICATION DEVICE

(57) Abstract

Known is a digital communication device, such as a pager, with an AFC loop. In order to avoid erroneous tuning in such a receiver to a strong adjacent channel, frequency offset compensation should be done over a limited range. A robust AFC control loop is provided by separating short term and long term frequency drift. Herewith, optimal short term compensation can be done. Alternatively, cost reduction can be achieved by allowing greater temperature and aging drifts.



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"Digital communication device"

The present invention relates to a digital communication device comprising a receiver having a mixer which is coupled to a local frequency generating arrangement, a demodulator which is coupled to the receiver, a microcontroller which is coupled to the demodulator being arranged for providing a frequency offset value being a difference between a frequency value representative of an output frequency of the local frequency generating arrangement and a frequency value representative of a desired tuning frequency, and frequency adjustment means for adjusting the frequency of the local frequency generating arrangement in dependence of the frequency offset value. Such a digital communication device can be a pager, or any other suitable digital communication device such as a cellular or cordless telephone, or the like. The receiver can be a super heterodyne receiver, a direct conversion quadrature receiver, or any other suitable receiver.

A digital communication device of this kind is known from the European Patent Application EP 0 735 675 A2. The known device comprises an automatic frequency control (AFC) loop for adjusting the frequency of a local oscillator in accordance with a frequency offset between a frequency of the local oscillator and a desired tuning frequency. In order to avoid erroneous tuning to a strong adjacent channel, in such communication devices frequency offset compensation should only be done in a limited range. The known communication device has a temperature sensor so as take into account temperature effects in the AFC control loop. Such a temperature sensor renders the communication device complicated. Besides, no measures are described for taking into account long term effects such as aging. Herewith, in the long run, the communication device can run out of its specifications.

It is an object of the present invention to provide a more robust digital communication device in which both the effects of long term and short term frequency drift effects are taken into account.

To this end the communication device according to the present invention is characterised in that the microcontroller is arranged for processing the frequency offset value such that long term frequency drift is separated from short term frequency drift, whereby the frequency adjustment means comprises a frequency adjustment reference value which is updated in accordance with the separated long term frequency drift. Herewith, under all circumstances maximum freedom is achieved for compensating short frequency drift such as temperature drift or drift caused by co-channel interference. Alternatively, cost reduction can be achieved by allowing greater temperature and aging drifts. The present invention is based upon the insight to adapt the frequency adjustment reference value over a relatively long period such that it follows the long term frequency drift such as drift caused by aging effects in components of the communication device, such as a reference crystal in the local frequency generating arrangement. Also incidents causing a similar effect as aging are compensated for. Such an incident can be a sudden change in parameter values of a crystal oscillator when the receiver is subjected to a shock, e.g., by being dropped. Such a quasi short term drift will initially add to the short term offset which may be partly compensated, but will eventually be fully compensated for because in the long run it is considered by the drift compensation mechanism as a long term drift effect.

Embodiments of a digital communication device according to the present invention are given in the dependent claims. Claim 2 achieves that in the factory the digital communication device is optimally aligned before being sold. Claim 3 achieves that a good separation is made between short term and long term drift, whereby short term averaging can be done over minutes and long term averaging can be done over months, for instance. Claim 4 achieves that a non-linear relationship or any other predetermined relationship between reference and control value is taken into account, whereas claim 5 gives an advantageous embodiment thereof. Claim 6 achieves proper measurement of the frequency offset values in a pager. Generally, the demodulator is a digital demodulator. Such demodulators have the capability to provide frequency offset values.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein

Fig. 1 schematically shows a functional block diagram of a digital communication device according to the present invention,

Fig. 2 shows a mixed hardware/software implementation of frequency

adjustment according to the present invention,

Fig. 3 shows a frequency offset diagram as a function of time so as to illustrate the operation of the frequency adjustment,

Fig. 4 shows a flow-chart for long term offset compensation,

Fig. 5 shows a flow-chart for short term offset compensation, and

Fig. 6 shows registers to further illustrate the operation of the frequency adjustment.

Throughout the figures the same reference numerals are used for the same features.

Fig. 1 schematically shows a functional block diagram of a digital communication device 1 according to the present invention. The digital communication device 1 comprises an antenna 2 coupled to a receiver having a mixer. Such a structure of a communication device is well-known and is not shown in detail here. The digital communication device 1 further comprises a local oscillator 3 as a local frequency generating arrangement coupled to the mixer in the reception path. A demodulator 4 is coupled to an output of the mixer (not shown). The local frequency generating arrangement can be any other suitable arrangement such as a controlled synthesizer or the like. Preferably quadrature demodulation is done so that quadrature signals I and Q are available. The demodulator 4 provides demodulated data dta and a frequency offset value offs. Such a demodulator 4 is well-known per se. The frequency offset value offs is a difference between a frequency value representative of an output frequency of the local oscillator 3 and a frequency value representative of a desired tuning frequency. In the event the digital communication device 1 is a selective pager, such a pager can be tuned to a particular channel. It should be prevented that the pager or any other suitable digital communication device would tune to an undesired neighbouring channel. Such a situation could occur when a frequency adjustment loop would not function properly. According to the present invention a very robust frequency adjustment loop (Automatic Frequency Adjustment AFC) is provided, particularly eliminating long term drift effects caused by aging, for instance, but also eliminating short term drift effects caused by short term temperature variations, for instance. Such an AFC is done by separating long term and short term frequency drift. Frequency adjustment means are provided comprising a frequency adjustment reference value REF which is updated in accordance with the separated long term frequency drift. Separation is done in a microcontroller 5 having RAM, EEPROM

and ROM memory, and registers, by separate averaging of the measured frequency offset value offs. The structure of such a microcontroller is well-known and is not shown in detail here. Short term averaging is done in process block 6 and long term averaging is done in block 7, on a minute and a month basis, for instance. The respective averaging results are combined in combining block 8. For obtaining a proper AFC initial value initial alignment is done in the factory by inserting an alignment value ALGN in the combining block 8. Preferably, alignment is done such that the AFC is set midway the AFC range. Furthermore, the offset is adjusted to zero. Alternatively, alignment can be done by using a software routine achieving that the offset is set to zero without any further manual alignment. An output of the combining block 8 is supplied to a digital-to-analog converter 9 of which an output voltage is fed to a filter 10 comprising a resistor 11, a capacitor 12 and a coil 13. At an other side, the coil 13 is coupled to a junction of a capacitor 14 and a varicap 15, the series arrangement of which being connected parallel to a crystal 16 in the local oscillator 3.

Fig. 2 shows a mixed hardware/software implementation of frequency adjustment according to the present invention. A frequency offset detector 20 is shown which is comprised in the demodulator 4. A register 21 stores a present AFC control value steering the digital-to-analog converter. Any new frequency offset offs detected by the frequency offset detector 20 is supplied to a new AFC control value register 22 after having been converted to an AFC value in the offset-to-AFC-value converter 23. At regular time intervals, the short term compensation loop, indicated with short term compensation block 24, updates the present AFC control value as stored in the register 21. An offset compensation limit as stored in a register 25 is used as an input for this update. The latter value is determined by the particular application and is a fixed value. In a message pager, for instance, the offset compensation limit value could be 2 kHz. The AFC reference value REF as stored in a register 26 and provided by the long term compensation loop, indicated with long term compensation block 27, is used as a second input for updating the present AFC control value as stored in the register 21. The reference value REF represents the aging information as generated by the long term compensation loop. As described, the AFC reference value REF is updated at a very low rate. As an example, assume a present AFC control value of 4 kHz and an actual receiver offset of 3 kHz. Then, the detector 20 detects a new offset offs of -1 kHz. After addition in the adder block 28, the new AFC control value becomes +3 kHz which corresponds to the actual frequency offset of the digital communication device 1. Although the maximum offset compensation range of the short term compensation loop is limited to 2 kHz, it can compensate for 3 kHz because its limit is

related to the AFC reference value REF. In the example given, a long term offset of +2.5 kHz is assumed to have been detected over a large period, a couple of months, for instance.

Fig. 3 shows a frequency offset diagram as a function of time t so as to illustrate the operation of the frequency adjustment. The frequency offset offs, shown in ppm, caused by aging is according to the curve 30. Just below the curve 30 an updated reference value REF is shown as a function of the time t. Further shown are a positive offset compensation limit curve 31 and a negative offset compensation limit curve. As can be seen, according to the present invention, full positive and negative compensation ranges R1 and R2 are available in the course of time. The AFC reference value REF is stored in RAM. This reference value stored in RAM is copied to EEPROM at regular intervals, once a day, for instance. This is not to loose the long term reference value in the event the supply voltage drops below the RAM retention voltage. Such a situation could occur when changing the supply battery of the digital communication device 1. The compensation range needs to be limited because the receiver could erroneously tune to a strong adjacent channel. Without separated long term/short term offset compensation as according to the present invention, either one of the positive or negative offset ranges would run out of a compensation range in the course of time.

Fig. 4 shows a flow-chart for long term offset compensation. In block 40, the offset offs is measured. In block 41, the measured offset value offs is converted to an AFC value new-AFC. In block 42, the new AFC value new-AFC is stored in the register 22. In block 43 the AFC reference value REF becomes AFC reference value REF + ((new-AFC minus AFC reference value)/2^n), n being an integer value. In block 45, the determination of the new long term AFC value is terminated. The above computation is the arithmetic average of the new AFC control value over a long period such as a one month period.

Fig. 5 shows a flow-chart for short term offset compensation. In block 50, the offset offs is measured and in block 51 converted to a new AFC value new-AFC which is stored in the register 22 in block 52. In block 53, the stored new AFC control value is subtracted from the AFC reference value REF and the result of this subtraction is compared with an offset compensation limit off_lim. In block 54, the present AFC control value := the new AFC control value if the comparison result is negative. In block 55, the present AFC control value becomes the sum of the AFC reference value REF and the offset compensation limit off_lim. In block 56, the short term compensation is terminated.

Fig. 6 shows registers to further illustrate the operation of the long term frequency adjustment. The present AFC reference value pres_REF, 6 bit, for instance, is

stored as the most significant bits of a long register, 21 bits, for instance. The initial value of pres_REF can be set at factory alignment. The other 15 bits are set to zero at the initial AFC alignment. A 6 bit calculated new average AFC value new_AFC is subtracted from the present AFC value pre_AFC. The difference is added to the least significant part of the 21 bits register. Herewith, the difference DIF divided by 2^{15} is added to the reference value so that it will take 2^{15} calculations before the average difference is added to or subtracted from the reference value. So, assuming one calculation per minute, it takes 32768 minutes or approximately 23 days before a persistent difference has reached the reference value. During this long period any temperature variations will have been averaged out so that true aging compensation is achieved.

In view of the foregoing it will be evident to a person skilled in the art that various modifications may be made within the spirit and the scope of the present invention as hereinafter defined by the appended claims and that the present invention is thus not limited to the examples provided.

CLAIMS:

1. A digital communication device comprising a receiver having a mixer which is coupled to a local frequency generating arrangement, a demodulator which is coupled to the receiver, a microcontroller which is coupled to the demodulator being arranged for providing a frequency offset value being a difference between a frequency value representative of an output frequency of the local frequency generating arrangement and a frequency value representative of a desired tuning frequency, and frequency adjustment means for adjusting the frequency of the local frequency generating arrangement in dependence of the frequency offset value, characterised in that the microcontroller is arranged for processing the frequency offset value such that long term frequency drift is separated from short term frequency drift, whereby the frequency adjustment means comprises a frequency adjustment reference value which is updated in accordance with the separated long term frequency drift.

2. A digital communication device according to claim 1, wherein the frequency adjustment reference value is initially aligned such that the frequency offset becomes zero.

3. A digital communication device according to claims 1 or 2, wherein the short term drift and the long term drift are determined by respective averaging of the frequency offset value over averaging periods of substantially different lengths.

4. A digital communication device according to claim 3, wherein a frequency adjustment control value and the frequency adjustment reference value are related to each other in accordance with a predetermined function.

5. A digital communication device according to claim 4, wherein the predetermined function is stored as a look-up table in the microcontroller.

6. A digital communication device according to claim 3, wherein the digital communication device is a pager, whereby the frequency offset value is determined at a synchronisation word received by the pager.

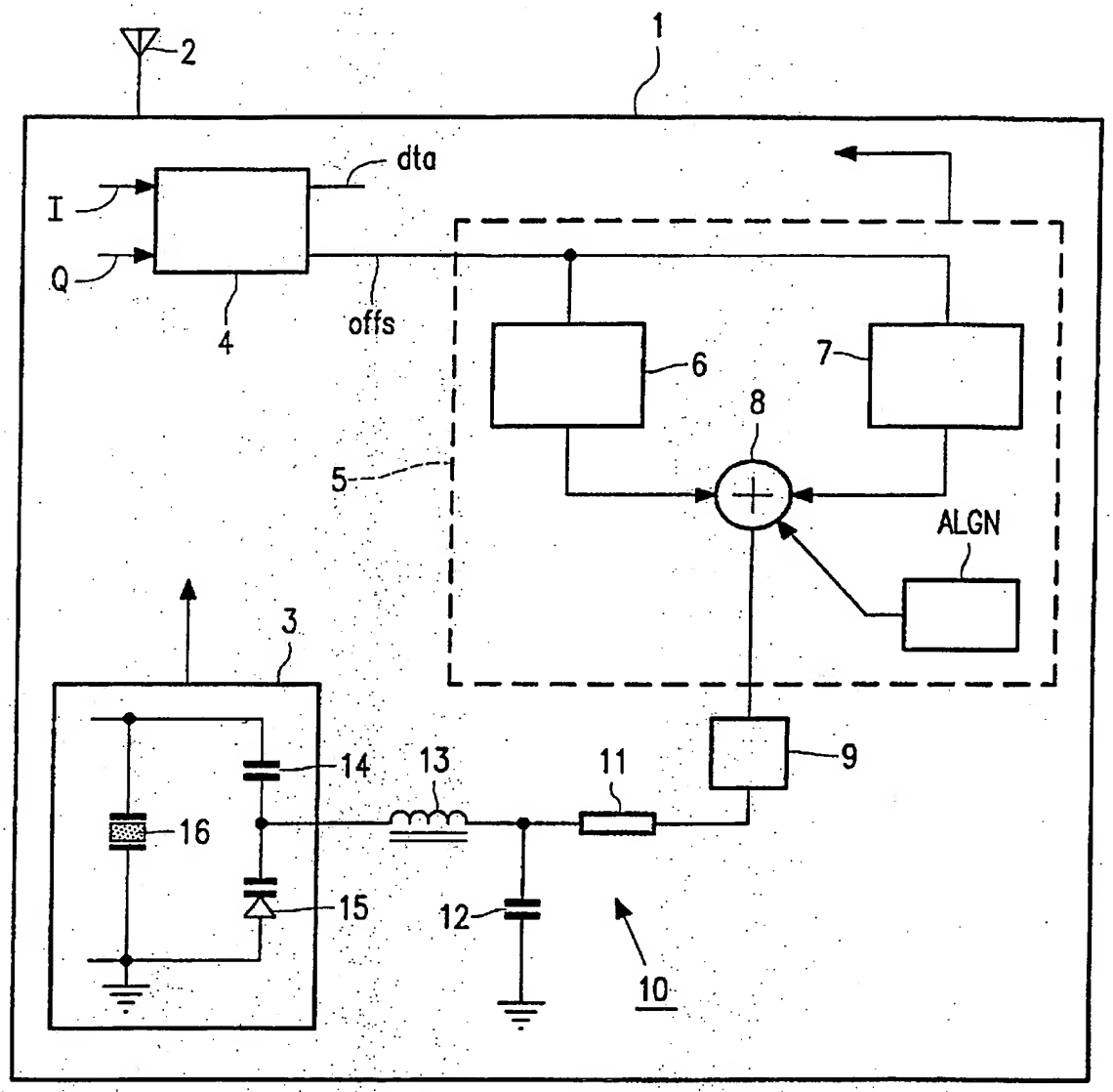


FIG. 1

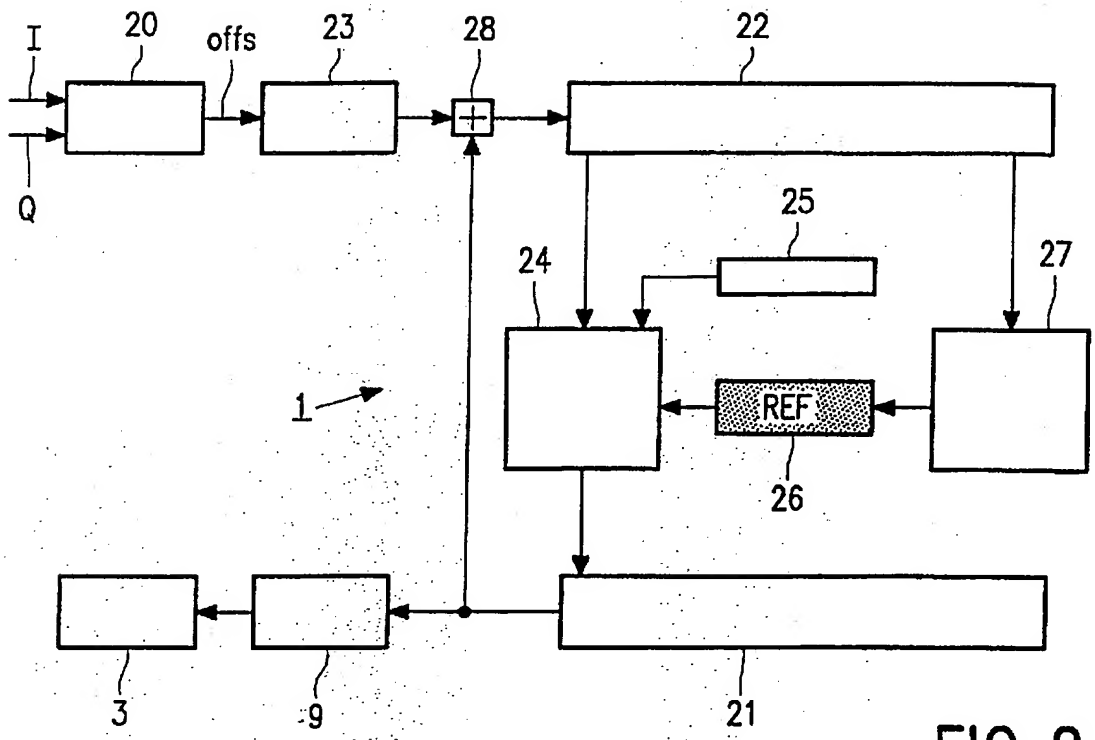


FIG. 2

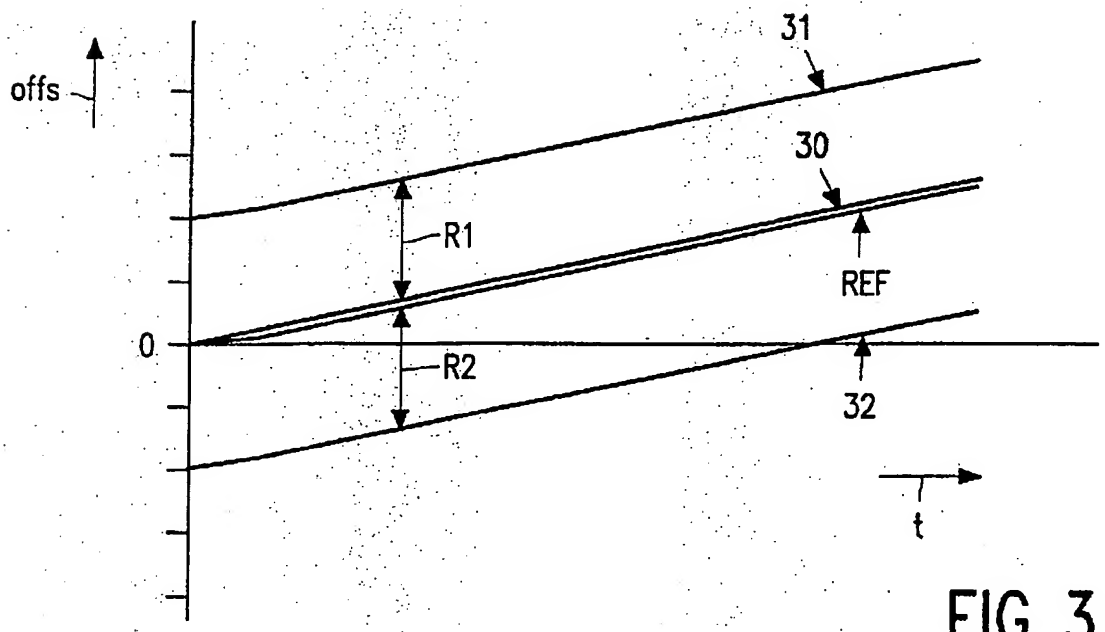


FIG. 3

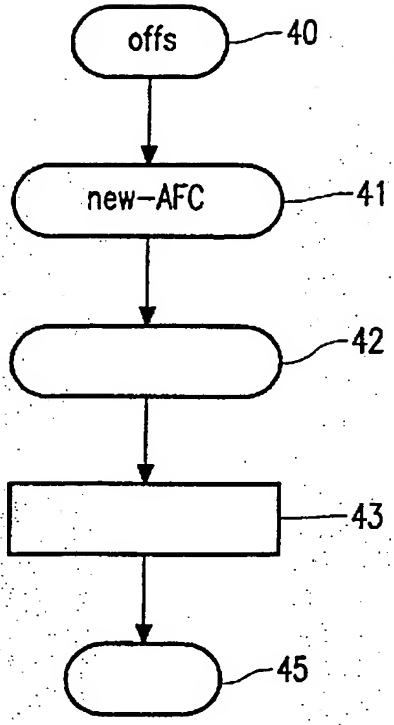
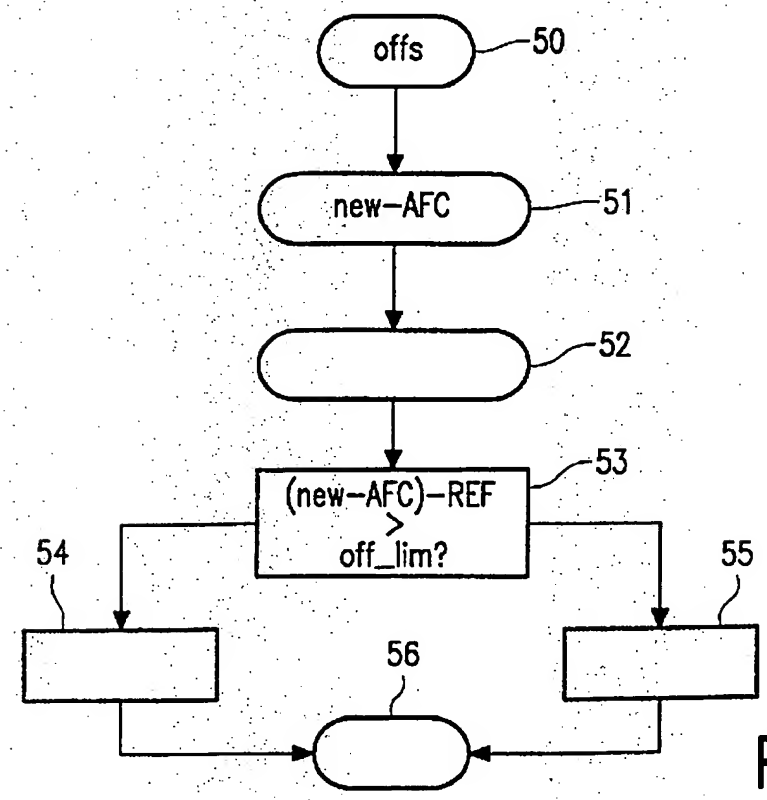

offs
40
new–AFC
41
42
43
45

FIG. 4


offs
50
new–AFC
51
52
(new–AFC)–REF
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off_lim?
53
54
55
56

FIG. 5

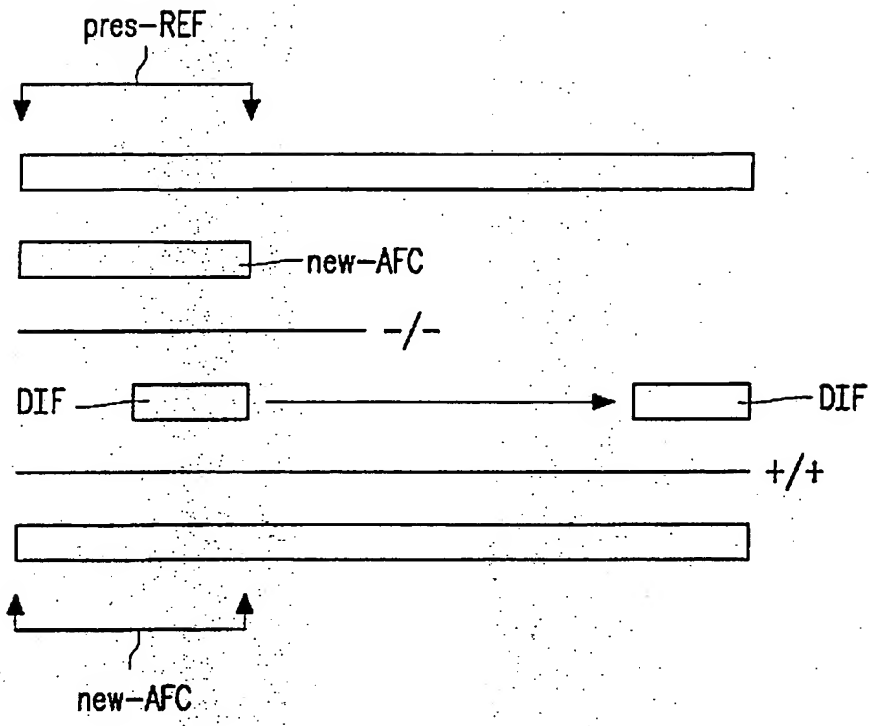

FIG. 6